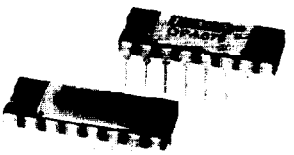
BURR-BROWN®



OPA675
OPA676

ABRIDGED DATA SHEET

For Complete Data Sheet
Call FaxLine 1-800-548-6133
Request Document Number 10864

Wideband Switched-Input OPERATIONAL AMPLIFIER

FEATURES

- FAST SETTLING: 9ns (1%)
- WIDE BANDWIDTH: 185MHz (A_V = 10)
- LOW OFFSET VOLTAGE: ±250µV
- TWO LOGIC SELECTABLE INPUTS
- FAST INPUT SWITCHING: 8ns (TTL)
- 16-PIN DIP PACKAGE

APPLICATIONS

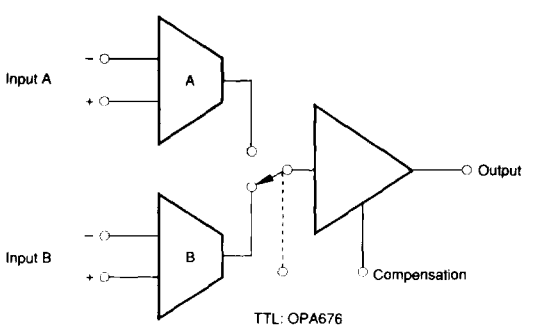
- PROGRAMMABLE-GAIN AMPLIFIER
- FAST 2-INPUT MULTIPLEXER
- SYNCHRONOUS DEMODULATOR
- PULSE/RF AMPLIFIERS
- VIDEO AMPLIFIERS
- ACTIVE FILTERS

DESCRIPTION

The OPA675 and OPA676 are wideband monolithic operational amplifiers with two independent differential inputs. Either input can be selected by an external logic signal. The OPA675 is compatible with ECL logic while the OPA676 is TTL compatible. Both amplifiers are externally compensated and feature very fast input selection speed: ECL = 4ns, TTL = 6ns. This amplifier features fully symmetrical differential inputs due to its "classical" operational amplifier circuit architecture. Unlike "current-feedback" amplifier designs, the OPA675/676 may be used in all op amp applications requiring high speed and precision.

Low distortion and crosstalk make these amplifiers suitable for RF and video applications.

The OPA675 and OPA676 are available in KG (0°C to +70°C) and SG (–55°C to +125°C) grades. All grades are packaged in a 16-pin DIP.



TTL: OPA676
ECL: OPA675

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SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±5VDC, R_L = 150Ω, and T_A = +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	OPA675/676JG, SG MIN	OPA675/676JG, SG TYP	OPA675/676JG, SG MAX	OPA675/676KG MIN	OPA675/676KG TYP	OPA675/676KG MAX	UNITS
INPUT NOISE[1]								
Voltage: f_O = 10Hz	R_S = 0Ω		27			*		nV/√Hz
f_O = 100Hz			10			*		nV/√Hz
f_O = 1kHz			3.8			*		nV/√Hz
f_O = 10kHz			2.6			*		nV/√Hz
f_O = 100kHz			2.4			*		nV/√Hz
f_B = 10Hz to 10MHz			7.9			*		µVrms
Current: f_O = 10Hz to 1MHz			2.7			*		pA/√Hz
OFFSET VOLTAGE[1]								
Input Offset Voltage	V_{CM} = 0VDC		±500	±2mV		±250	±1mV	µV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±3	±10		±1	±5	µV/°C
Supply Rejection	$\pm V_{CC}$ = 4.5V to 5.5V	65	86		70	*		dB
BIAS CURRENT[1]								
Input Bias Current	V_{CM} = 0VDC		23	35		*	30	µA
OFFSET CURRENT[1]								
Input Offset Current	V_{CM} = 0VDC		0.8	5		*	*	µA
INPUT IMPEDANCE[1]								
Differential			4k || 2			*		Ω || pF
Common-Mode			10^5 || 5			*		Ω || pF
INPUT VOLTAGE RANGE[1]								
Common-Mode Input Range		±1.25	±2.5		*	*		V
Common-Mode Rejection	V_{IN} = ±0.5VDC, V_O = ±1.25V	75	100		85	*		dB
OPEN LOOP GAIN, DC[1]								
Open-Loop Voltage Gain		65	70		*	*		dB
FREQUENCY RESPONSE								
Closed-Loop Bandwidth	Gain = +2V/V		100			*		MHz
	Gain = +5V/V		145			*		MHz
	Gain = +10V/V		185			*		MHz
	Gain = +50V/V		60			*		MHz
Crosstalk	Gain = +10V/V, f = 100kHz		–100			*		dBC[2]
	f = 1MHz		–80			*		dBC
	f = 10MHz		–68			*		dBC
	f = 100MHz		–35			*		dBC
Harmonic Distortion: 10MHz	G = +10V/V, R_L = 50Ω, V_O = 0.5Vp-p							
	Second Harmonic		–61			*		dBC
	Third Harmonic		–73			*		dBC
Full Power Response	V_O = 2.5Vp-p, Gain = +10V/V	25	44		30	*		MHz
Slew Rate	Gain = +10V/V	200	350		240	*		V/µs
Settling Time: 1%			9			*		ns
0.1%	Gain = +10V/V		15			*		ns
0.01%	0.625V Output Step		25			*		ns
INPUT SELECTION[3]								
Transition Time	ECL: OPA675		5			*		ns
50% In to 50% Out	TTL: OPA676		7.5			*		ns
DIGITAL INPUT								
TTL Logic Levels: V_{IL}	Logic "LO"	0		+0.8	*		*	V
V_{IH}	Logic "HI"	+2.0		+5	*		*	V
I_{IL}	Logic "LO", V_{IL} = 0V		–0.05	–0.2		*	*	mA
I_{IH}	Logic "HI", V_{IH} = +2.7V		1	20		*	*	µA
ECL Logic Levels: V_{IL}	Logic "LO"	–1.81		–1.475	*		*	V
V_{IH}	Logic "HI"	–1.15		– 0.88	*		*	V
I_{IL}	Logic "LO", V_{IL} = –1.6V		–50	–100		*	*	µA
I_{IH}	Logic "HI", V_{IH} = –1.0V		–50	–100		*	*	µA
RATED OUTPUT								
Voltage Output	R_L = 150Ω	±2.1	±2.6		*	*		V
	R_L = 50Ω	+1.25	+1.8		*	*		V
		–0.95	–1.1		–1.0	*		V
Current Output			±30			*		mA
Output Resistance	1MHz, Open-Loop, C_C = 5pF		5			*		Ω
Load Capacitance Stability	Gain = +2V/V		50			*		pF
Short Circuit Current	Continuous to Gnd		+45			*		mA
			–25			*		mA

* Same specifications as for JG.

SPECIFICATIONS (CONT)

ELECTRICAL

At V_{CC} = ±5VDC, R_L = 150Ω, and T_A = +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	OPA675/676JG, SG			OPA675/676KG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY								
Rated Voltage	±V_{CC}		5			*		VDC
Derated Performance	±V_{CC}	4.5		6.5	*		*	VDC
Current, Quiescent	I_O = 0mADC		22	30		*	*	mA
TEMPERATURE RANGE								
Specification	Ambient Temp JG, KG	0		+70	*		*	°C
	SG	–55		+125				°C
Operating:	Ambient Temp JG, KG, SG	–55		+125	*		*	°C
θ_{JA}			125			*		°C/W

* Same specifications as for JG.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

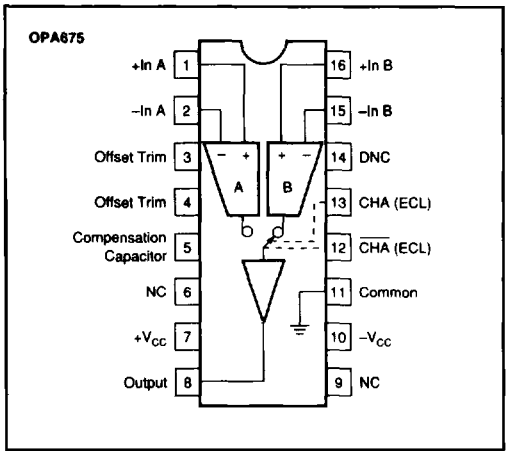
At V_{CC} = ±5VDC, R_L = 150Ω, and T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

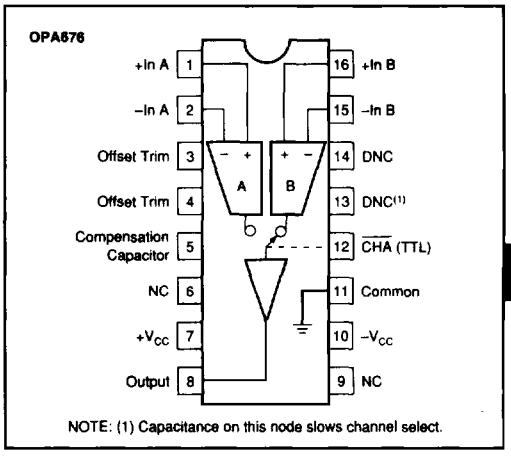
PARAMETER	CONDITIONS	OPA675/676JG, SG			OPA675/676KG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE								
Specification	Ambient Temp JG, KG	0		+70	*		*	°C
	SG	–55		+125				°C
OFFSET VOLTAGE								
Average Drift	T_A = T_{MIN} to T_{MAX}		±3	±10		±1	±5	µV/°C
Supply Rejection	±V_{CC} = 4.5V to 5.5V	60	85		65	*		dB
BIAS CURRENT								
Input Bias Current	V_{CM} = 0VDC		29	50		*	*	µA
OFFSET CURRENT								
Input Offset Current	V_{CM} = 0VDC		0.8	10		*	*	µA
INPUT VOLTAGE RANGE								
Common-Mode Input Range		±2.0	±2.3		*	*		V
Common-Mode Rejection	V_{IN} = ±0.5VDC, V_O = ±1.25V	60	80		65	*		dB
OPEN LOOP GAIN, DC								
Open-Loop Voltage Gain		60	68		63	69		dB
DIGITAL INPUT								
TTL Logic Levels: V_{IL}	Logic "LO"	0		+0.8	*		*	V
V_{IH}	Logic "HI"	+2.0		+5	*		*	V
I_{IL}	Logic "LO", V_{IL} = 0V		–0.08	–0.4		*	*	mA
I_{IH}	Logic "HI", V_{IH} = +2.7V		5	50		*	*	µA
ECL Logic Levels: V_{IL}	Logic "LO"	–1.81		–1.475	*		*	V
V_{IH}	Logic "HI"	–1.15		–0.88	*		*	V
I_{IL}	Logic "LO", V_{IL} = –1.6V		–50			*		µA
I_{IH}	Logic "HI", V_{IH} = –1.0V		–50			*		µA
RATED OUTPUT								
Voltage Output	R_L = 150Ω	±2.0	±2.5		*	*		V
	R_L = 50Ω	+1.25	+1.6		*	*		V
		–0.8	–1.0		–0.9	*		V
POWER SUPPLY								
Current, Quiescent	I_O = 0mADC		25	35		*	*	mA

* Same specifications as for JG.

NOTES: (1) Specifications are for both inputs (A and B). (2) dBC = Level referred to carrier-input signal. (3) Switching time from application of digital logic signal to input signal selection.

PIN CONFIGURATIONS





NOTE: (1) Capacitance on this node slows channel select.

PIN ASSIGNMENTS: OPA675

1	+In A	16	+In B
2	–In A	15	–In B
3	Offset Trim	14	DNC
4	Offset Trim	13	CHA (ECL)
5	Compensation Capacitor	12	CHA (ECL)
6	NC	11	Common
7	$+V_{CC}$	10	$-V_{CC}$
8	Output	9	NC

DNC = Do Not Connect NC = No Internal Connection

PIN ASSIGNMENTS: OPA676

1	+In A	16	+In B
2	–In A	15	–In B
3	Offset Trim	14	DNC
4	Offset Trim	13	DNC
5	Compensation Capacitor	12	CHA (TTL)
6	NC	11	Common
7	$+V_{CC}$	10	$-V_{CC}$
8	Output	9	NC

DNC = Do Not Connect NC = No Internal Connection

ABSOLUTE MAXIMUM RATINGS

Supply	±7VDC
Differential Input Voltage	Total V_{CC}
Input Voltage Range (Analog and Digital)	$\pm V_{CC}$
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit to Ground (+25°C)	Continuous to ground
Junction Temperature	+175°C

ORDERING INFORMATION

OPA675 ( ) ( )
OPA676 ( ) ( )

Basic Model Number
Performance Grade Code
J, K: 0°C to +70°C
S: –55°C to +125°C
Package Code
G: 16-pin Ceramic DIP

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA675/76JG	16-Pin Hermetic DIP	109
OPA675/76SG	16-Pin Hermetic DIP	109
OPA675/76KG	16-Pin Hermetic DIP	109

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.